TECHNISCHE UNIVERSITÄT DRESDEN

Center for Information Services and High Performance Computing (ZIH)

HPC Power Measurements Procurement Guidelines

Building Energy Efficient High Performance Computing: 4th Annual EE HPC WG Workshop

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Phase 1 Requirements and Accuracy Tests

- Requirements
  - Full system energy accounting
  - 2% accuracy
  - Min. 1 sample/s
  - Granularity: node level
  - Correct energy calculation based on power samples

- Reference measurements to evaluate accuracy of energy accounting
  - Use professional power meters (ZES LMG 450)
  - Use synthetic idle/busy-loop-benchmark to trigger worst case scenarios (find frequency with highest aliasing effects)

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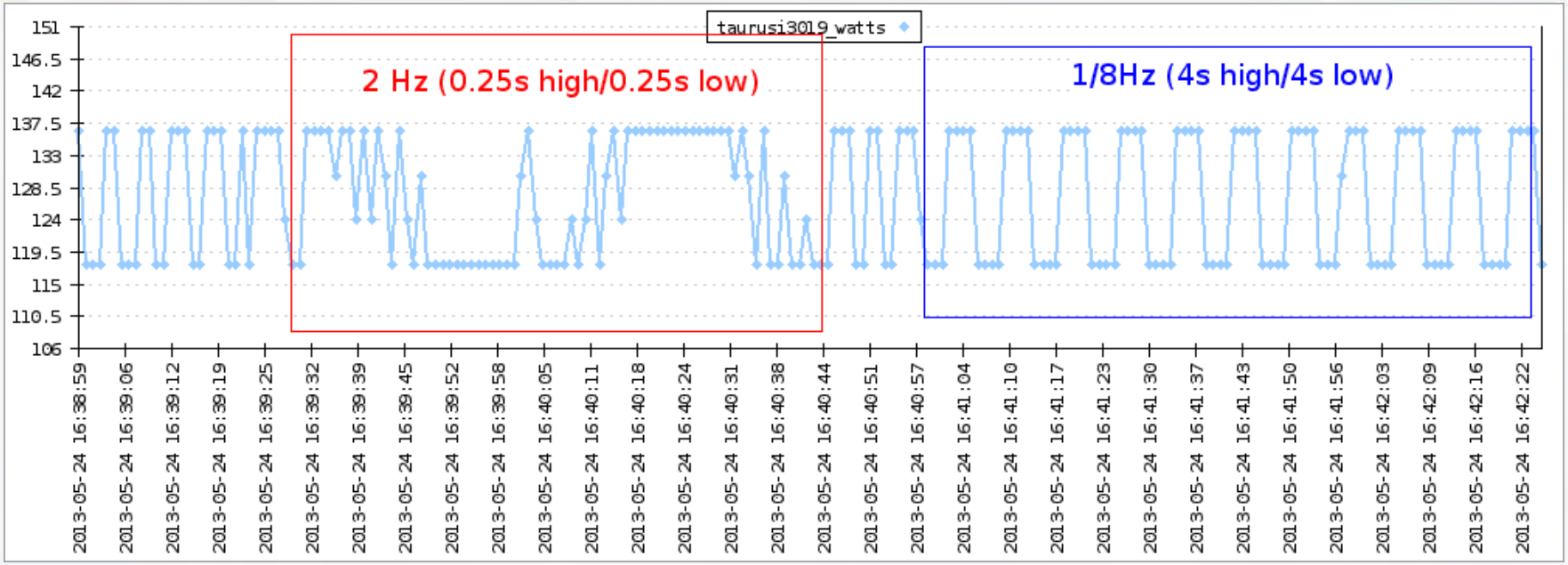
Reference Measurement: 8 DC 54V Channels per Chassis

Energy Correctness Test with Synthetic Benchmark



- Accuracy acceptance test:
  - Submitting 5 identical jobs with ‘worst case properties’
  - Accounting results of -49% to +36% compared to reference measurement
- Multiple errors in energy calculation code of Slurm (now mostly fixed)
- Aliasing effects already in data coming from BMC
- High idle power variations – node measurement calibration disastrous
- IPMI limitation of 8 bit per value: power measurement granularity of 2 to 7 W

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HPC Power Measurements Usage Models

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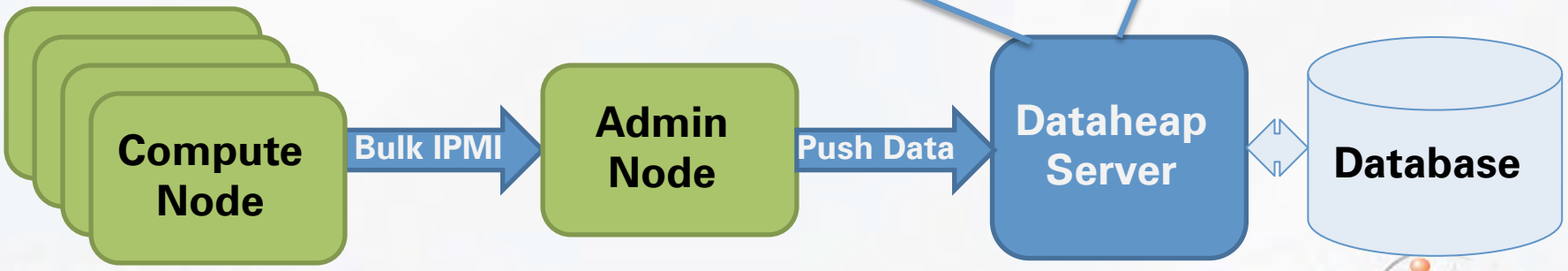
Power Measurement Data Management: Dataheap

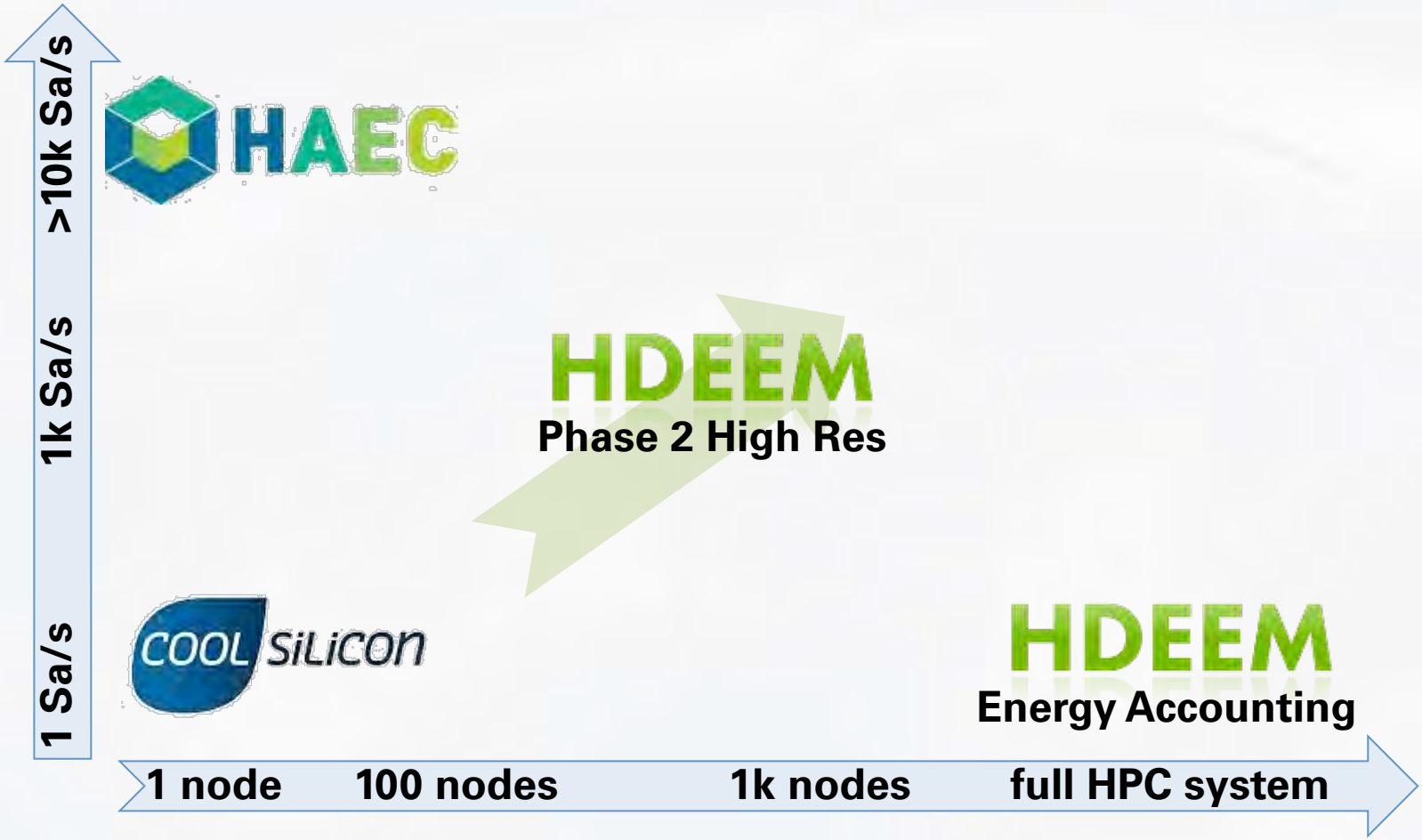
Live viewers, e.g. Website

Post-Mortem Analysis, e.g.

- Get energy of job
- Get energy for node
- Analyze long term energy savings since optimization
- Websites



Power Measurement Projects at TU Dresden



The Classics: Live System View

The Classics: History View

- Power at >= 1 sample/s, temperature at > 1 sample/min
- All components: nodes, switches, storage etc.
- Full history, not data reduction/dumping

The Advanced: Performance + Efficiency Analysis at Scale

Trace View - Taurus:/scratch/jschuch/cosmo/3400778/scorep-20131028_1717_3631706115203084/traces.otf2* - Vampir

File Edit Chart Filter Window Help

Timeline

575 s 580 s 585 s 590 s 595 s 600 s 605 s 610 s 615 s 620 s

Master thread:0
Master thread:2
Master thread:4
Master thread:6
Master thread:8
Master thread:10
Master thread:12
Master thread:14
Master thread:16
Master thread:18
Master thread:20
Master thread:22
Master thread:24
Master thread:26
Master thread:28
Master thread:30
Master thread:32
Master thread:34
Master thread:36
Master thread:38
Master thread:40
Master thread:42
Master thread:44
Master thread:46
Master thread:48
Master thread:50
Master thread:52
Master thread:54
Master thread:56
Master thread:58
Master thread:60
Master thread:62

node taurusi1121, Values of Counter "node/watts" over Time

Watts: 340, 320, 300, 280, 260

Function Summary

All Processes, Number of Invocations per Function

2,359,296	__advection_ift_fd...MOD_advfd4_addflux
2,359,296	__advection_ift_fd...advfd4_computeflux
1,966,080	__numeric_utilities_rk_MOD_udsdx
196,608	__advection_ift_fd...D_advfd4_updaterho
196,608	__advection_ift_fd4...OD_advfd4_initblock
196,608	__src_sbm_MOD_sbmfd4_sum_single
12,724	MPI_Isend
10,720	__environment_MOD_getbuf
10,720	__environment_MOD_putbuf
10,720	MPI_Wait
10,720	MPI_Recv
10,624	__time_utilities_MOD_get_timings
3,968	__environment_MOD_exchg_boundaries
3,072	__meteo_utilities_MOD_satad
2,004	MPI_Irecv
1,152	__src_advection_rk_MOD_adv_upwind3_lat
1,152	__src_advection_rk...OD_adv_upwind3_lon

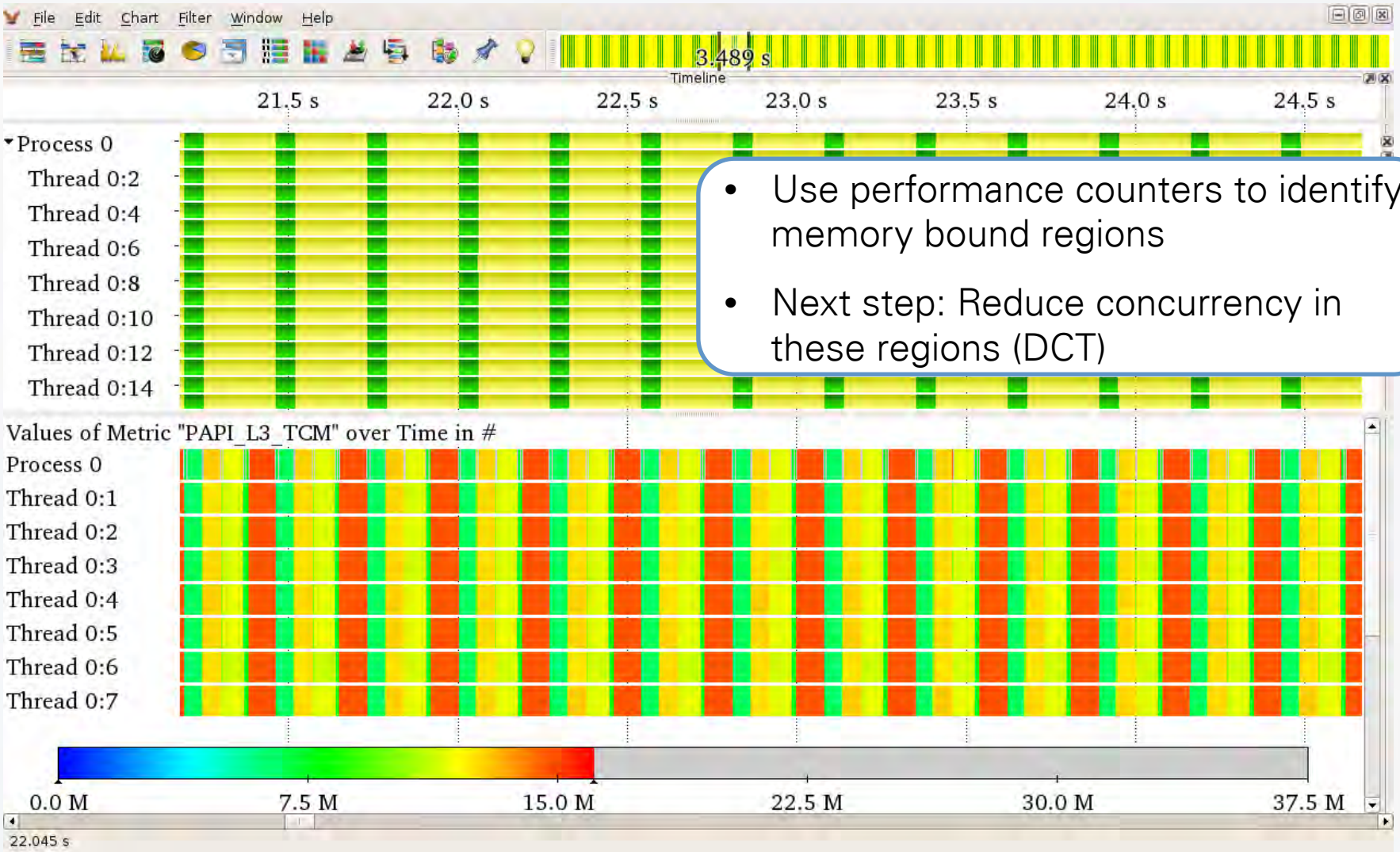
Context View

Process Timeline

Property	Value
Display	Process Timeline
Type	Function
Location	Master thread:0
Function	__advection_ift_fd4_mod_MOD_advfd4_addflux
Function Group	Application
Interval Begin	577.995598 s
Interval End	577.995637 s
Duration	38.049 µs
Source Code	Advection_IfT_fd4.f90:509

- COSMO on 4 nodes of HRSK-II phase 1 (dual socket Sandy Bridge-EP)

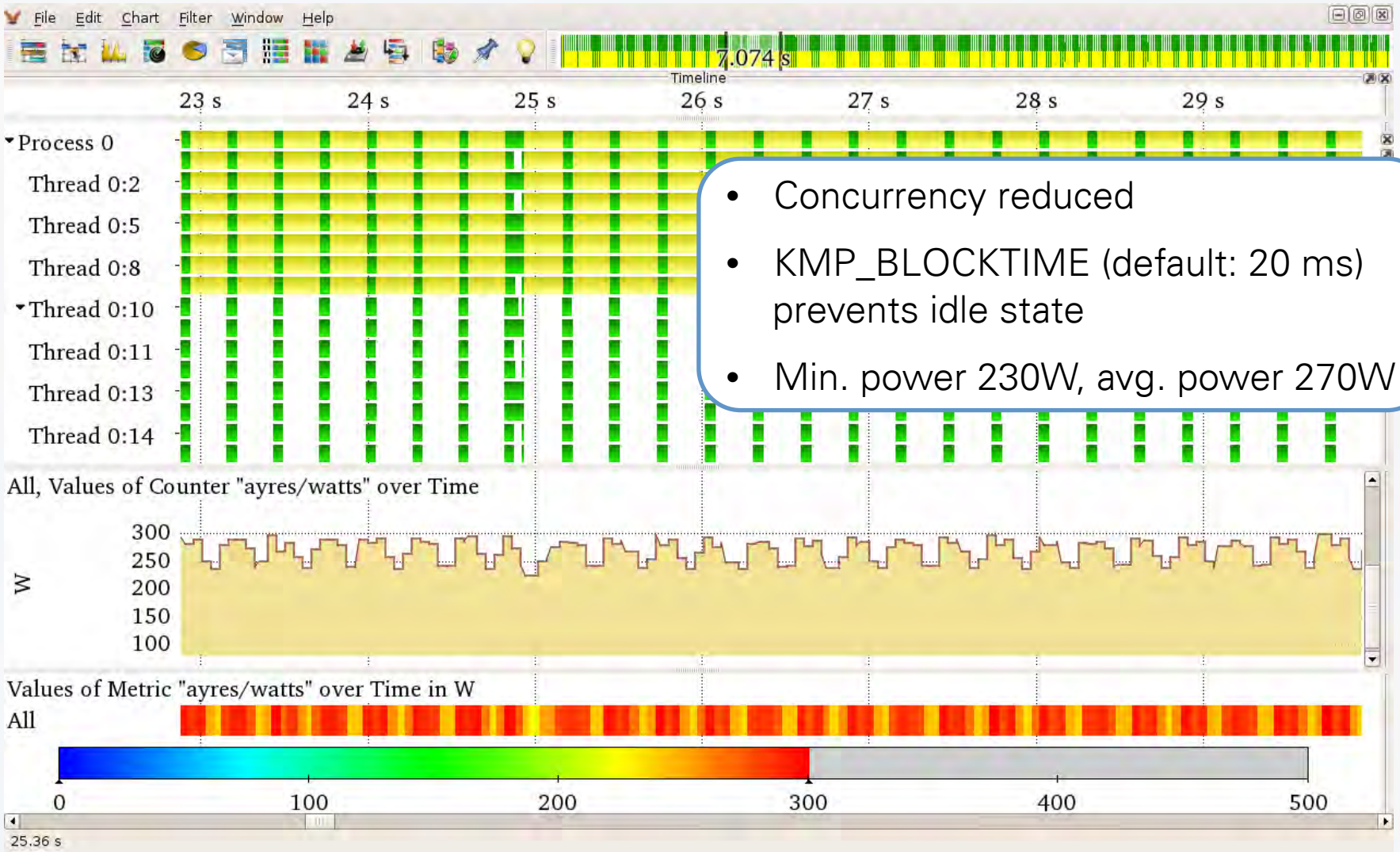
Combining Performance Analysis and Energy Optimization



- Use performance counters to identify memory bound regions
- Next step: Reduce concurrency in these regions (DCT)

NAS Parallel Benchmark sp.C on Intel Xeon E5-2670

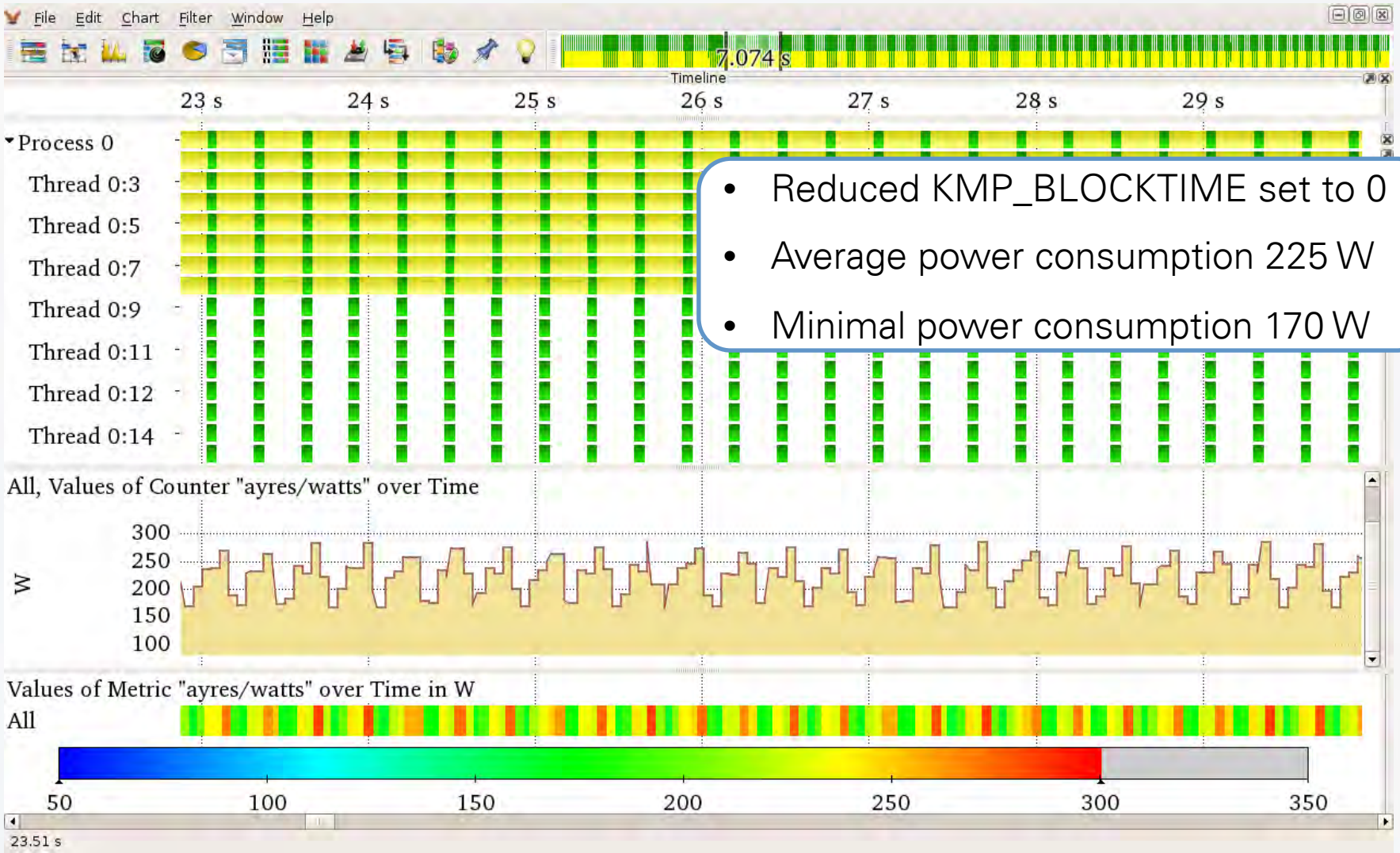
Combining Performance Analysis and Energy Optimization



- Concurrency reduced
- KMP_BLOCKTIME (default: 20 ms) prevents idle state
- Min. power 230W, avg. power 270W

NAS Parallel Benchmark sp.C on Intel Xeon E5-2670

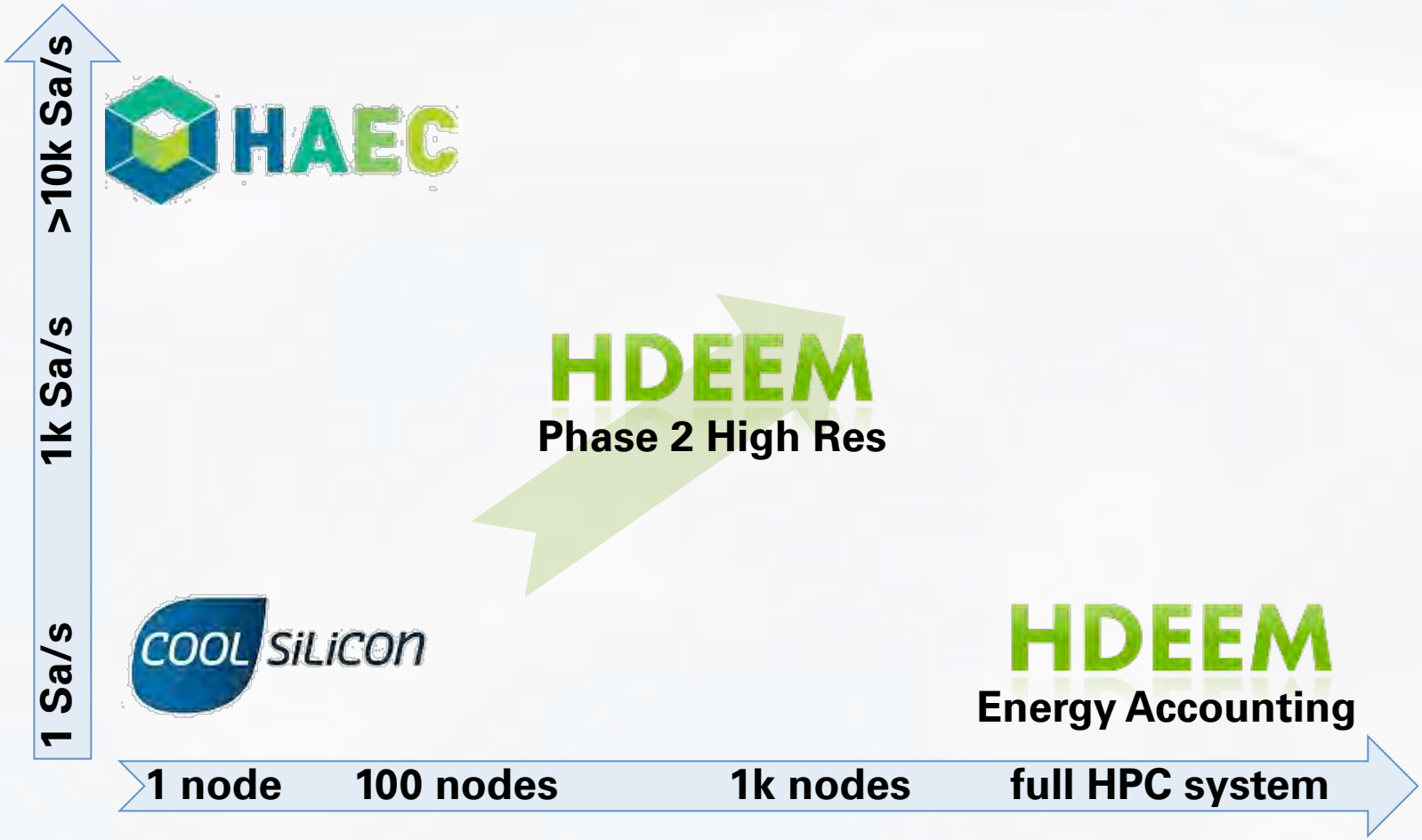
Combining Performance Analysis and Energy Optimization



- Reduced KMP_BLOCKTIME set to 0
- Average power consumption 225 W
- Minimal power consumption 170 W

NAS Parallel Benchmark sp.C on Intel Xeon E5-2670

Power Measurement Projects at TU Dresden

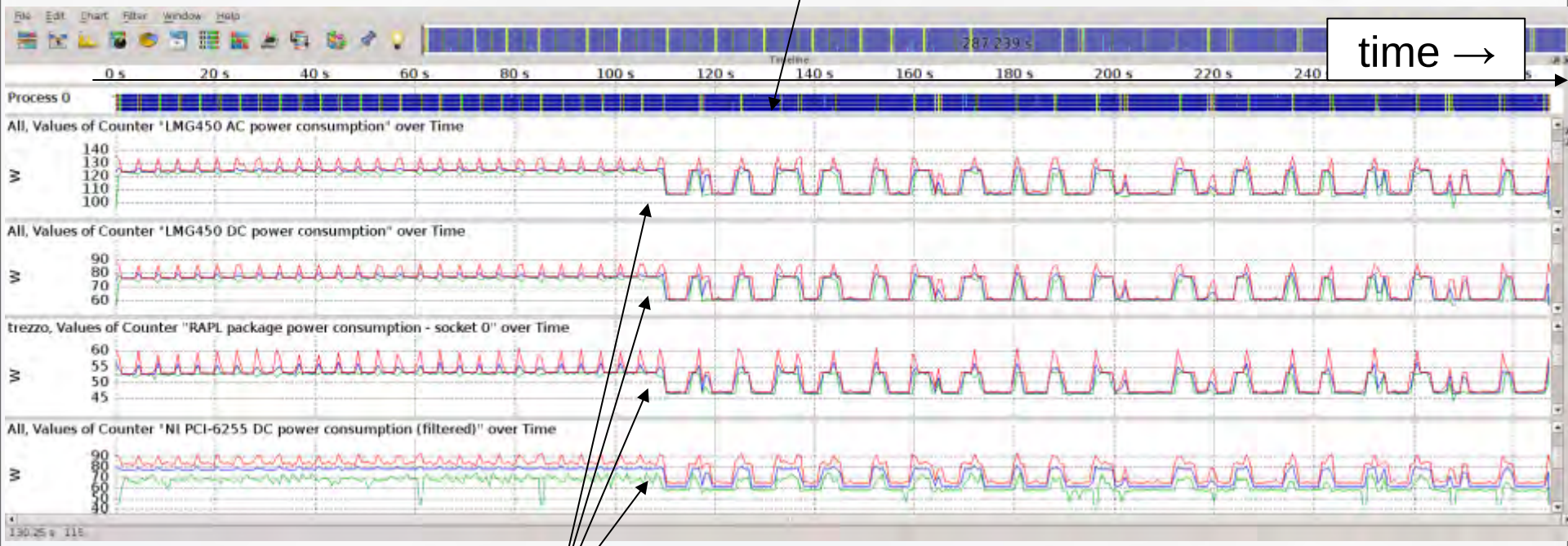


Combining Performance and Energy Efficiency Analysis

- SPEC OMP2001 (applu)
- How much power does my system consume at any given time during application execution?

application activity

time →



four different power-measurements

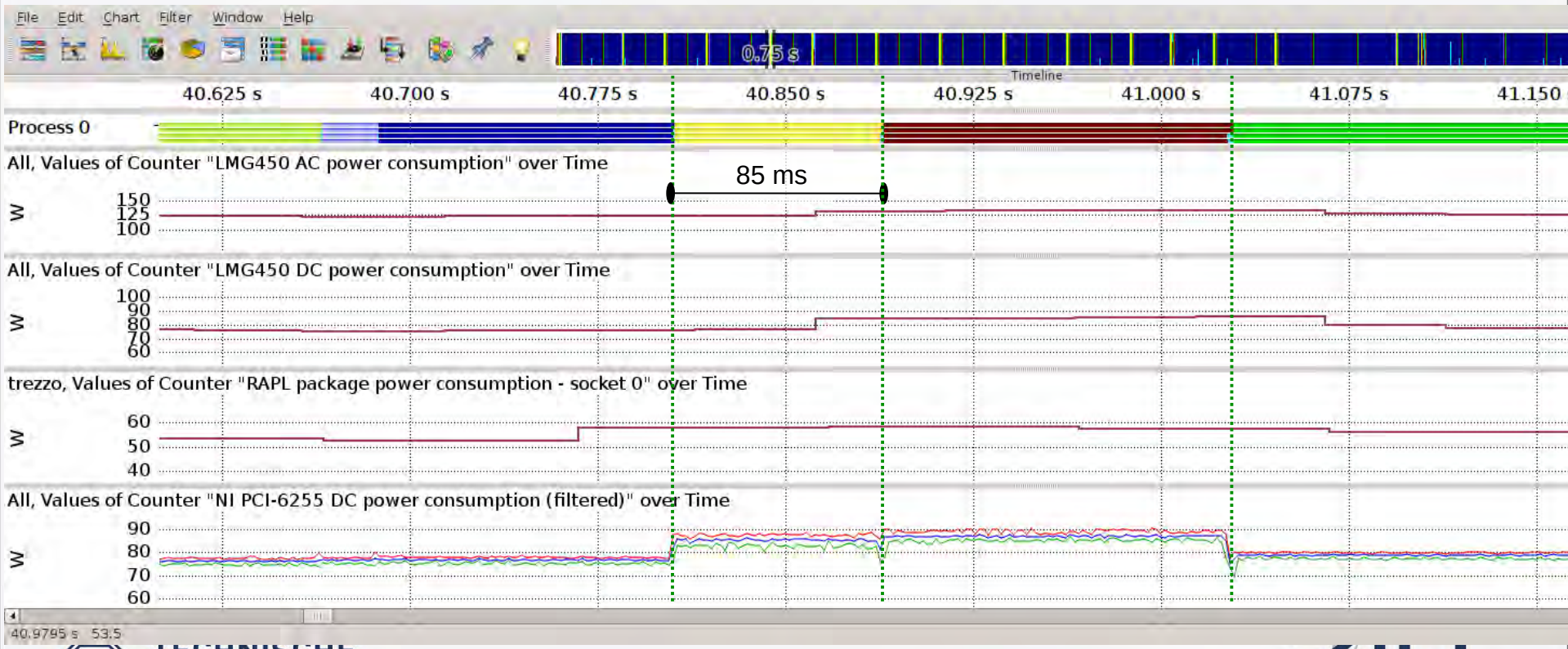
— maximum

— average

— minimum

Combining Performance and Energy Efficiency Analysis (2)

- Temporal granularity does matter when analyzing short code paths
  - LMG450 (AC and DC): 20 Sa/s
  - RAPL: 10 Sa/s (maximum 1 kSa/s*)
  - Hall sensor / NI (DC): 200 kSa/s (with 4.5 kHz low-pass filter)



Combining Performance and Energy Efficiency Analysis (3)

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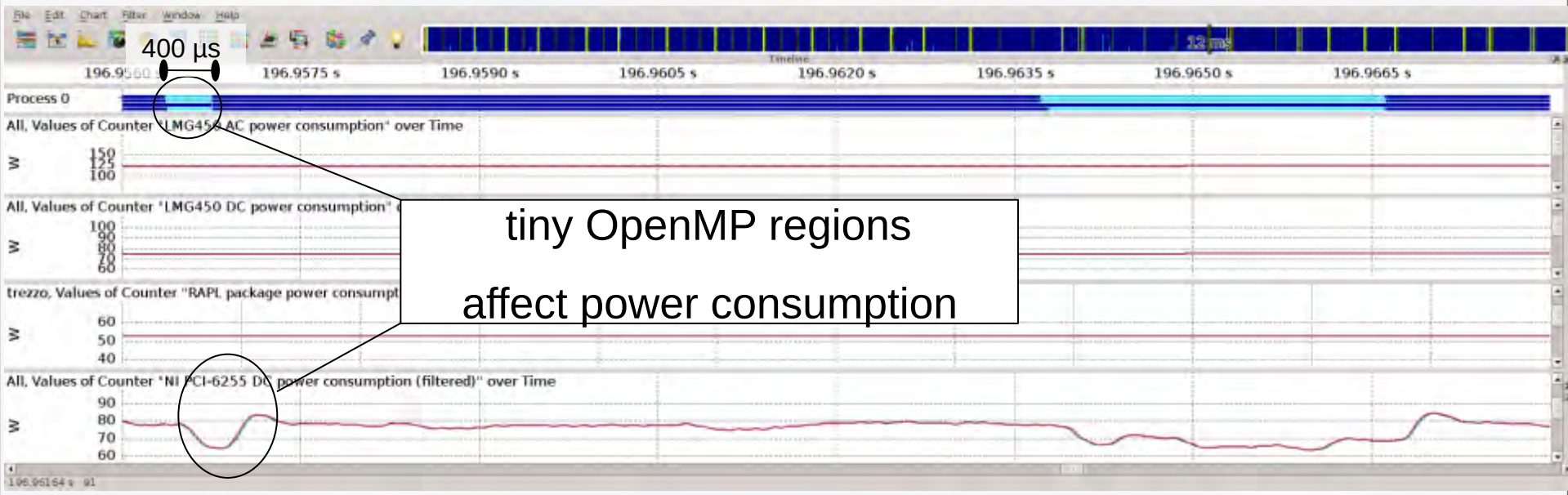
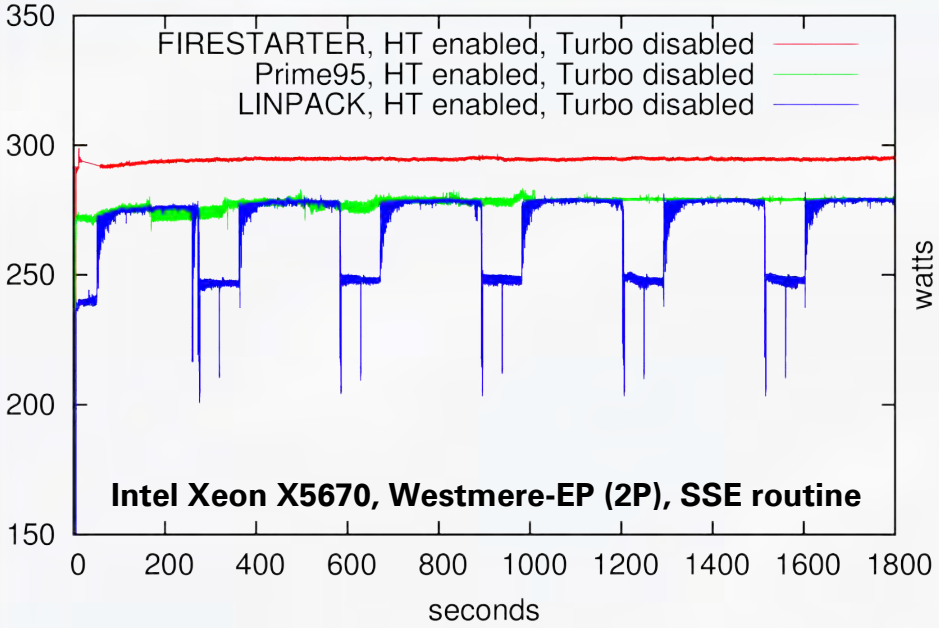
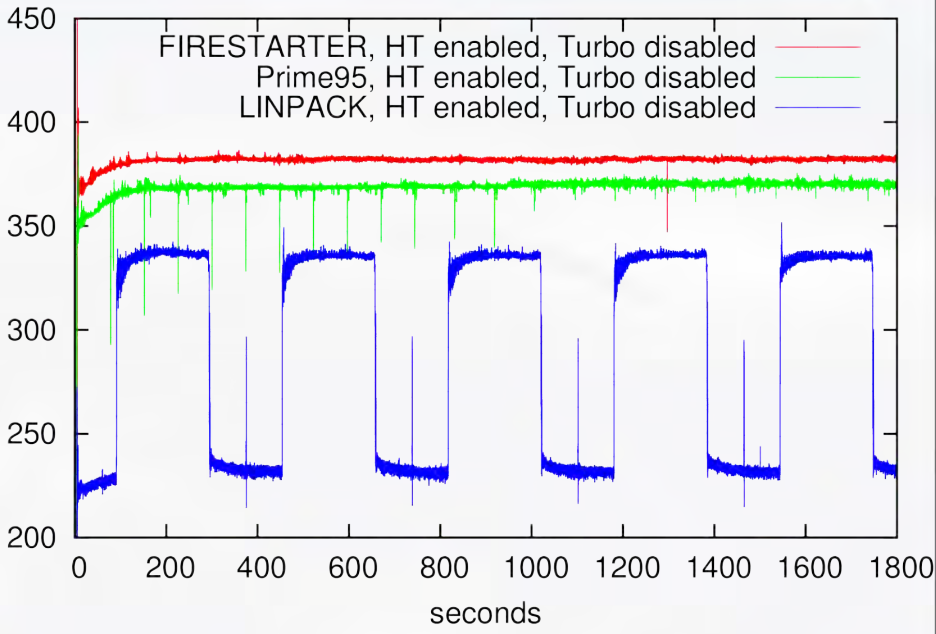


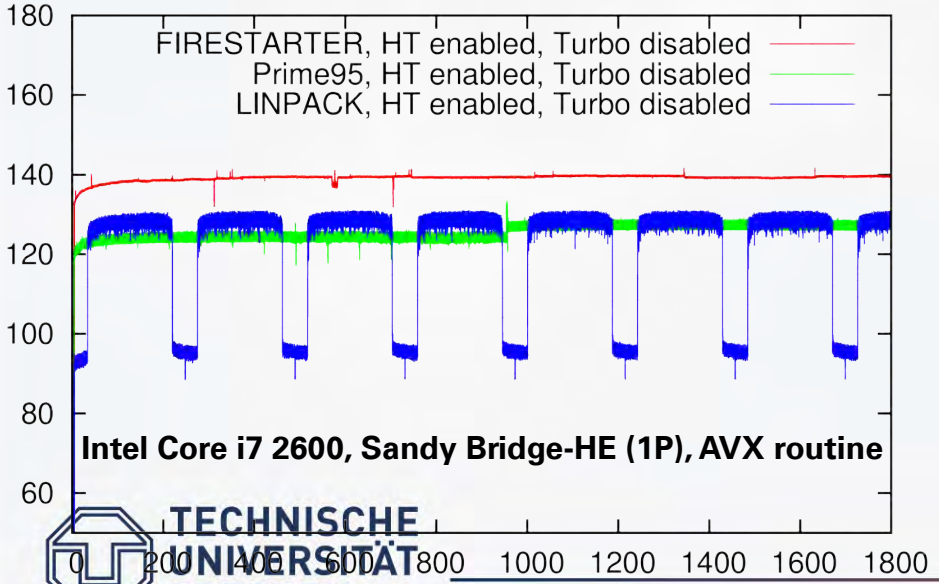
Thank you!

FIRESTARTER: A Processor Stress Test Utility





Intel Xeon E5-2670, Sandy Bridge-EP (2P), AVX routine



http://tu-dresden.de/zih/firestarter/

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Sustainability through energy efficiency. The region "Silicon Saxony" acted on this maxim and founded the Leading Edge Cluster "Cool Silicon - Energy Efficiency Innovations from Silicon Saxony".

The Leading Edge Cluster Cool Silicon

- is aiming at providing a technological basis for increasing the energy efficiency in the information and communications technology sector.
- is assuring Germany and Europe a leading role in the key technology of "energy efficiency in the information technology sector".

Micro- and Nanotechnologies

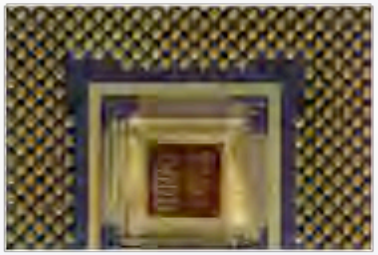
Communication Systems **Network Sensors**

Helping to solve a global conflict: The worldwide desire for free communication collides with global climate protection targets, in case the energy consumption of communications technology keeps expanding at its current pace.

Cool Silicon - Areas

Area 1
Micro- und Nanotechnologies

The core objective of the Area 1 project partners is the development of basis technologies, analysis and production methods for the production of energy efficient electronics and their application in order to decrease the energy consumption of computer systems.

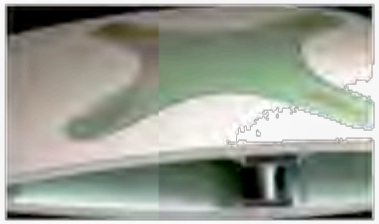


Area 2
Communication Systems

In Area 2, the research and development projects are focussing on the improvement of energy efficiency in communications infrastructures and mobile devices.

Area 3
Network Sensors

The project CoolSensorNet is the Lead Project of Area 3. It conducts research on the whole electronic chain's specific requirements, including sensors, analog electronics, A-D converters, processor systems and the telemetry unit.



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