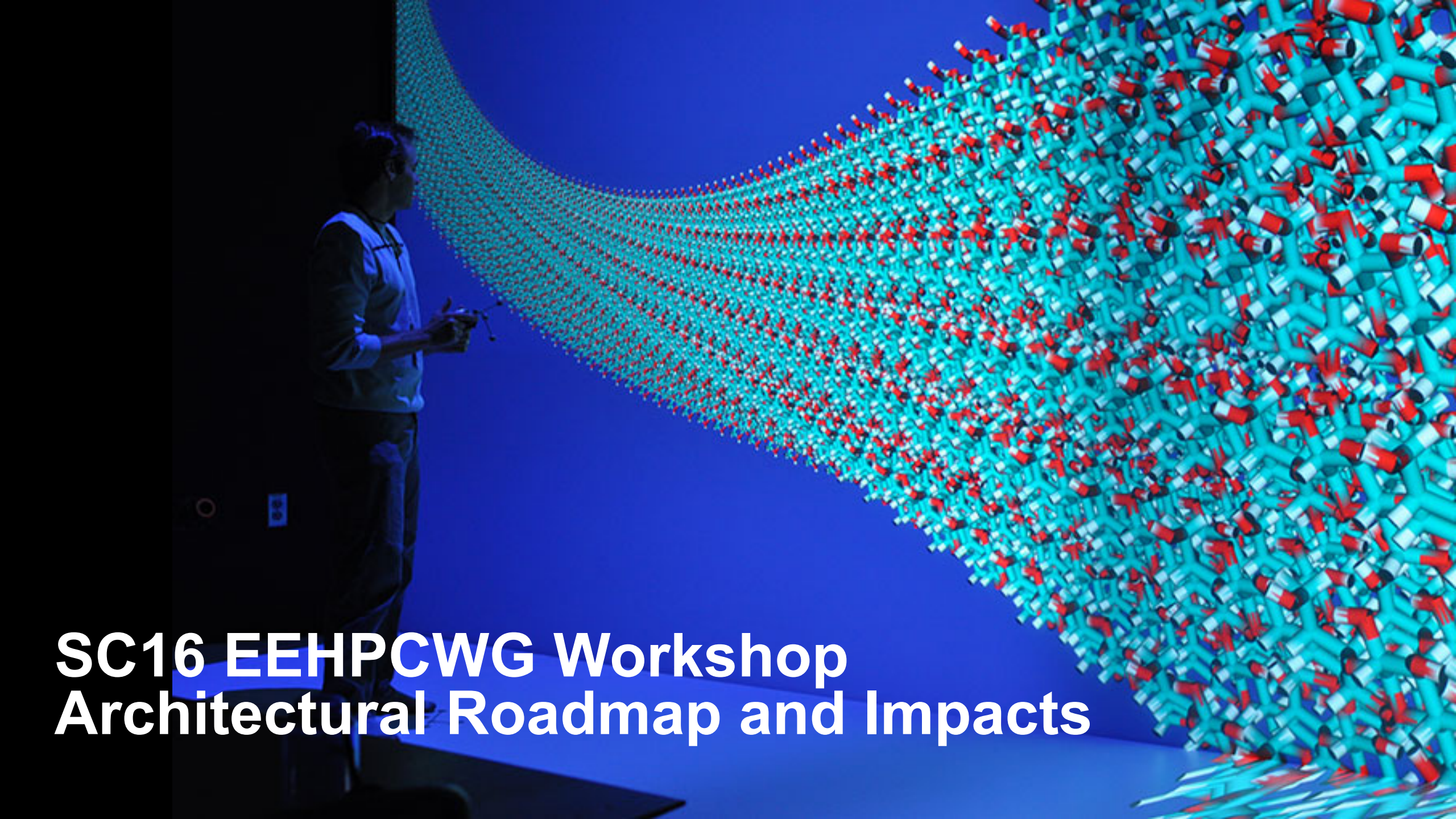
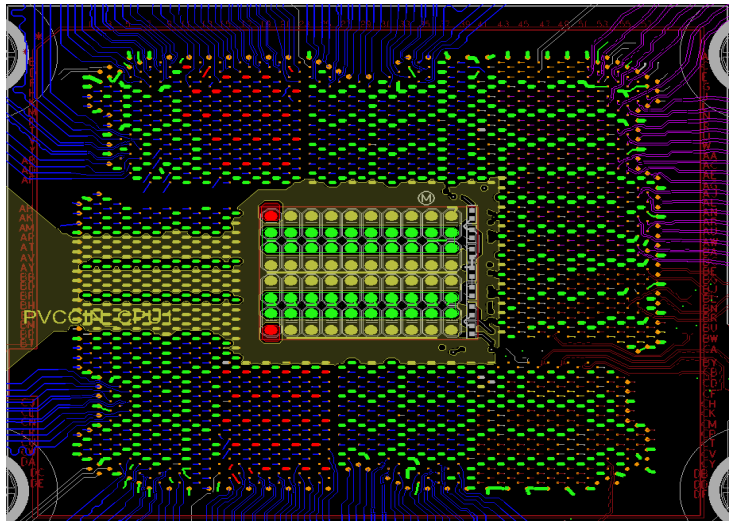
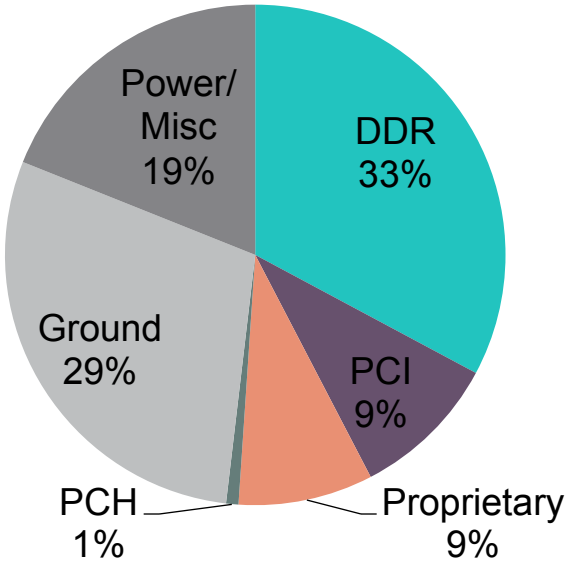


SC16 EEHPCWG Workshop
Architectural Roadmap and Impacts

System Ratios – Can the tendency be reversed?

Can we still afford I/O?





Interface	pins	%	bandwidth	Bw/pin
DDR 2400	660	33%	76.8	**0.116**
PCI Gen3	192	10%	40	**0.208**
Proprietary	175	9%	38.4	**0.219**
PCH	16	1%	3.93	**0.246**
Ground	587	29%		
Misc/Power	381	19%		

Today's optical technology:

1200$ / 100Gbps optical cable @ ~4 watts

or 12$ per Gbps and 40 pJ/bit

At Exascale: ~1B$ and >10MW (only for cabling)

Panelists

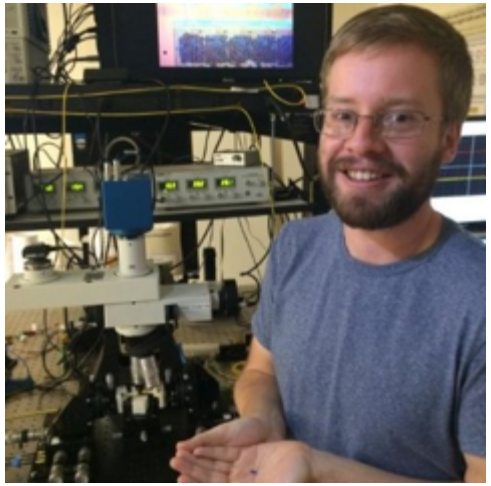
Al Gara

Intel Fellow & Intel® Xeon Phi™ Chief Architect

Keren Bergman

Charles Batchelor Professor and Chair of Electrical Engineering at Columbia University.

Director of the Columbia Nano Initiative



Mark Wade

Chief Scientist, Ayar Labs

Moderators:
Nicolas Dubé, Chief Technologist, Advanced Development Group, HPE
James Laros, Crossroads Chief Architect, Sandia National Labs