Embedded Technologies for Supercomputers

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Power is leading constraint for future performance growth.

Parallelism is growing at exponential rate.

Reliability going down for large-scale systems, but also to get more energy efficiency for small systems.

Memory Technology improvements are slowing down.

By 2018, cost of a FLOP will be less than cost of moving 5mm across the chip’s surface (locality will really matter).
HPC Market Overview

- High End Systems (>$1M)
- Most/all Top 500 systems
- Custom SW & ISV apps
- Technology risk takers & early adopters

IDC:
- 2005: $2.1B
- 2010: $2.5B

Volume Market
- Mainly capacity; <~150 nodes
- Mostly clusters; >50% & growing
- Higher % of ISV apps
- Fast growth from commercial HPC; Oil & Gas, Financial services, Pharma, Aerospace, etc.

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Total market >$10.0B in 2006
Forecast >$15.5B in 2011

HPC is built with a pyramid investment model
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Totally Bogus Prediction
IDC 2010 puts HPC market at $10B
1990s - R&D computing hardware dominated by desktop/COTS

- Had to learn how to use COTS technology for HPC
- Thomas Sterling’s “Beowulf Cluster”

2010 - R&D investments moving rapidly to consumer electronics/embedded processing

- Must learn how to leverage embedded/consumer processor technology for future HPC systems
- Think “Beowulf chip”

Image below From Tsugio Makimoto: ISC2006
Worldwide Intelligent Systems Unit Shipments Comparison - Embedded Systems vs. Mainstream Systems 2011 Share and Growth

Notes:
Size of bubble equals 2011 share of system shipments. Growth of cell phone system shipments is driven by smartphones and multi core processor designs.
Berkeley Sumbercomputer Predicts Your Doom

The University of California at Berkeley is rolling out a new breed of supercomputer, specially designed to predict the challenges presented by climate change, ultimately leading humanity to our doom and the computers to their rightful place as the masters of our earthly domain.

The idea driving the claim that supercomputers can be revolutionized is the radical notion that the computers themselves can control the climate and eventually lead to our own doom.
Consumer Electronics is the NEW Driver  
(and surprisingly aligned with our needs)

High Performance embedded is aligned with HPC

- HPC used to be performance without regard to power
- Now HPC is power limited (max delivered performance/watt)
- Embedded has always been driven by max performance/watt (max battery life) and minimizing cost ($1 cell phones)
- Now HPC and embedded requirements are aligned

Your “smart phone” is driving technology development

- Desktops are no longer in the drivers seat
- This is not a bad thing because high-performance embedded has longer track record of application-driven design
- Hardware/Software co-design comes from embedded design
- And its based on Specialization & use of SoC Design
Seymour Cray 1977: “Don’t put anything into a supercomputer that isn’t necessary.”

Mark Horowitz 2007: “Years of research in low-power embedded computing have shown only one design technique to reduce power: reduce waste.”
Building an SoC from IP Logic Blocks

Its legos with a some extra integration and verification cost
(Bill Dally’s “shopping List”) (anonymized price quotes)

Processor Core (ARM, Tensilica, MIPS deriv)
With extra “options” like DP FPU, ECC

NoC Fabric: (Arteris, Denali, other OMAP-4)

DDR3 1600 memory controller
(Denali / Cadence, SiCreations)
+ Phy and Programmable PLL

PCIe Gen3 Root complex

Integrated FLASH Controller

10GigE or IB DDR 4x Channel
Technology Continuity for A Sustainable Hardware Ecosystem

Very High Bandwidth Energy Efficient Photonic Interconnect

Floating Point Application Resilience Low Latency Memory and Interconnect

Ultra Energy Efficient Embedded System Platform

Energy Efficient Cloud Computing (Future Data Centers)

High Performance (Exascale) Computing System
Commoditization Strategies
(alternative approaches to amortize NRE)

Chip is the commodity (CPU and GPU w/1TF/chip in today’s tech)
- NRE: $1B to design each generation
- Mfr. Costs: $100/chip for 240mm and pennies for 7mm
- Most costs are in verification of full custom circuit design IP is mostly proprietary
- Design and Verification NRE is shared across products using that chip
- GPUs and CPUs specialized to different market (some waste)

ASICs using commodity IP (for a 0.5TF chip but more control of design)
- NRE: $2M in IP, $5M in assembly and verification, $2M for Mask + fab
- Mfr. Costs: $200/chip for initial 10K, and $100/chip beyond 50k chips
- NRE spread across 200k chips for large system is $50/chip
- Still have SW costs (but same baseline as commodity chip)
- No extra baggage in design (only include what you need for broad HPC application mix. Concentrate design + verification costs on small subset of design that needs to change)
Redefining “commodity”

- We cannot achieve energy efficiency by adding to the design (need way to include only what we need, and not what we don’t)
- Must use “commodity” technology to build cost-effective design
- The primary cost of a chip is development of the intellectual property
  - Mask and fab typically 10% of NRE in embedded
  - Design and verification dominate costs
  - SoC’s for high perf. consumer electronics is vibrant market for IP/circuit-design
  - Redefine your notion of “commodity”!

The ‘chip’ is not the commodity…

The stuff you put on the chip is the commodity

This is an alternative approach to leveraging economies of scale to achieve HPC goals
End

LBNL/Sandia Computer Architecture Laboratory
http://www.cal-design.org/